User Manual

GHD3440R

Three-phase 200V Gate Driver (with LDO)

Version: V1.0

Contents

1 Product overview

1.1 Introduction

GHD3440R is a three-phase medium-voltage high-speed gate drive IC, which is specially designed for driving double-N-channel VDMOS power transistor or IGBT in bridge circuits, and is suitable for application schemes for battery-powered DC brushless motors. The embedded typical dead time is 250ns. When the dead time of the MCU output signal is less than the embedded dead time, the actual dead time is the embedded dead time. On the contrary, when the dead time of the MCU output signal is greater than the embedded dead time, the actual dead time is the output dead time of MCU. The embedded VCC and VBS undervoltage protection functions can prevent the system from turning on the external power transistors at low driving voltage. The output of the high-side driving circuit and the output of the low-side driving circuit are controlled through input signals. The built-in LDO supports power supply for MCU and other control chips, and supports 3.3V or 5V voltage output through internal fuse tuning.

1.2 Main characteristics

- Operating supply voltage range: 5~20V
- Floating offset voltage: +200V
- Embedded minimum dead time:500ns
- Embedded VCC and VBS undervoltage protection
- Embedded straight-through prevention function
- Embedded input pull-down resistor
- Embedded output pull-down resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- Input and output in-phase
- Compatible with 3.3V/5V logic input
- Peak input current 1.1A@15V, 3.3nF load fall time 40ns
- Peak output current 0.9A@15V, 3.3nF load rise time 65ns
- LDO load capacity 60mA@15V
- Overtemperature protection threshold 151 ° C /131 ° C

1.3 Application scope

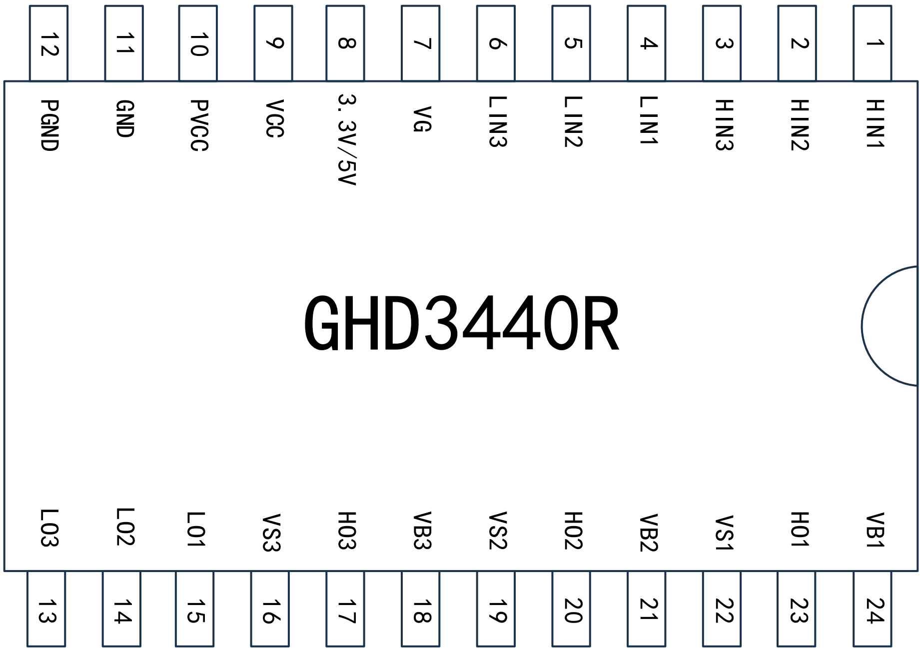
- Various tools based on DC brushless motors in battery-powered systems
- Electric tools, such as electric wrenches, electric screwdrivers, electric drills, and electric hammers

- Garden tools, such as lawn mowers, pruners, hedge trimmers, and chain saws
- Cleaning tools, such as electric cleaning brushes and vacuum cleaners

2 Pin information

2.1 Pin distribution

Figure 1 Distribution Diagram of GHD3440R Pins



2.2 Pin functional description

Table 1 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviations	Definitions
Pin Name	Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power supply pin
	I	Only input pin
	I/O	I/O pin

Table 2 Description of GHD3440R by Pin Number

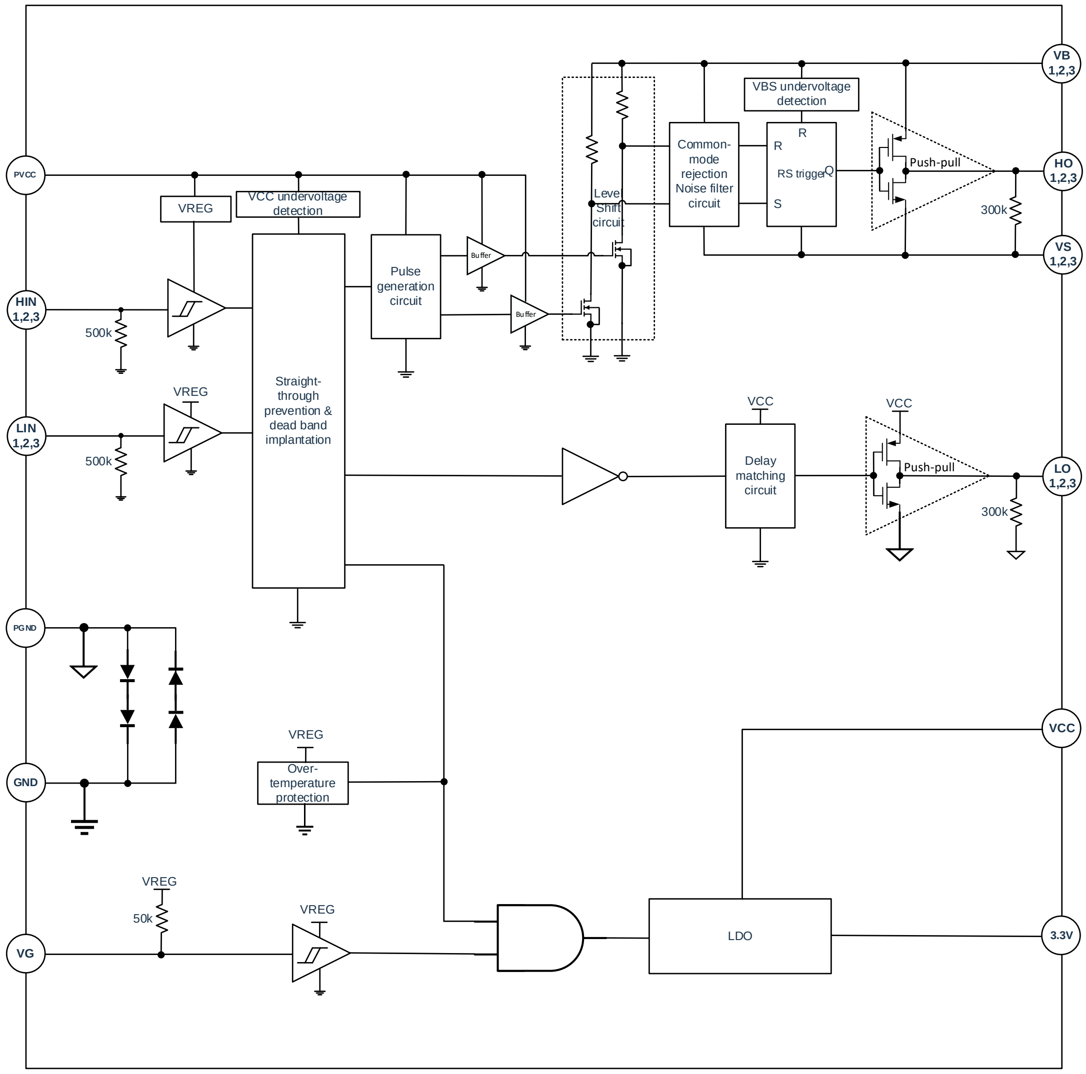
Name	Type	Functional Description	Pin sequence
HIN1	I	Phase-1 high-side input	1
HIN2	I	Phase-2 high-side input	2
HIN3	I	Phase-3 high-side input	3
LIN1	I	Phase-1 low-side input	4
LIN2	I	Phase-2 low-side input	5
LIN3	I	Phase-3 low-side input	6

Name	Type	Functional Description	Pin sequence
VG	P	LDO switch enable pin	7
3.3V/5V	P	3.3V/5V output pin (fuse adjustable)	8
VCC	P	Chip LDO power supply pin	9
VCC	P	Chip drive power supply pin	10
GND	P	Chip signal ground pin	11
PGND	P	Power ground	12
LO3	O	Phase-3 low-side output	13
LO2	O	Phase-2 low-side output	14
LO1	O	Phase-1 low-side output	15
VS3	P	Phase-3 high-side floating pin	16
HO3	O	Phase-3 high-side output	17
VB3	P	Phase-3 high-side bootstrap power pin	18
VS2	P	Phase-2 high-side floating pin	19
HO2	O	Phase-2 high-side output	20
VB2	P	Phase-2 high-side bootstrap power pin	21
VS1	P	Phase-1 high-side floating pin	22
HO1	O	Phase-1 high-side output	23
VB1	P	Phase-1 high-side bootstrap power pin	24

3 Block diagram logic

3.1 Internal block diagram

Figure 2 GHD3440R Internal Block Diagram



3.2 Logic truth value

Table 3 Logic Truth Value

OTP	VG	VCCUV	VBSUV	LIN	HIN	LO	HO	LDO
normal	normal	normal	normal	L	H	L	H	3.3V
normal	normal	normal	normal	H	L	H	L	3.3V
normal	normal	normal	normal	L	L	L	L	3.3V
normal	normal	normal	normal	H	H	L	L	3.3V

normal	normal	normal	UV	H&L	H&L	H&L	L	3.3V
normal	normal	UV	normal	H&L	H&L	L	L	3.3V
normal	L	normal	normal	H&L	H&L	H&L	H&L	0V
OVER	normal	normal	normal	H&L	H&L	L	L	0V

（1） VBS undervoltage will only set the HO output low.

（2） VCC undervoltage will set both LO and HO outputs low.

（3） The VG signal is pulled up to high by default, and the LDO output is turned off when the external pull-down is low.

（4） After the over temperature protection function is triggered, both the drive output and LDO output are turned off

4 Electrical characteristics

4.1 Recommended safe operating range

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 4 General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	-	105	℃
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$	$VS_{1,2,3}$+15	$VB_{1,2,3}$	V
$V_{LO1,2,3}$	Low-side output voltage	0	15	VCC	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	$VS_{1,2,3}$+5	$VS_{1,2,3}$+15	$VS_{1,2,3}$+20	V
$VS_{1,2,3}$	High-side floating offset relative voltage	GND-5	-	140	V
VCC	Supply voltage	5	15	20	V
V_{IN}	Input voltage (HIN1, 2, 3/LIN1, 2, 3)	0	-	5	V
VG	LDO switch enable pin	0	-	5	V
PGND	Power ground	-1.0	0	1.0	V

Note:

(1) When $VB_{1, 2, 3}$=$VS_{1, 2, 3}$+10, and $VS_{1, 2, 3}$ is (COM-5V)~(COM-VBS), the HO logic state is maintained. When $VS_{1, 2, 3}$ is (COM-5V) ~140V, HO operates normally.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

4.2 Absolute maximum rated value

T_A=25℃, all pins take GND as the reference points, unless otherwise specified.

Table 5 Power Consumption

Symbol	Description	Min	Max	Unit
P_D	Maximum power consumption	-	1.25	W

Note: At any time, the power consumption cannot exceed P_D. The calculation formula for the maximum power consumption at different ambient temperatures is: P_D=(150℃-T_A)/θ_{JA},

150℃ is the maximum operating junction temperature of the circuit, T_A is the operating ambient temperature of the circuit, and θ_{JA} is the thermal resistance of the package.

Table 6 Temperature Characteristics

Symbol	Description	Min	Max	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	75	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 7 Maximum Rated Voltage Characteristics

Symbol	Description	Min	Max	Unit
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$-0.3	$VB_{1,2,3}$+0.3	V
$V_{LO1,2,3}$	Low-side output voltage	-0.3	VCC+0.3	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	-0.3	225	V
$VS_{1,2,3}$	High-side floating offset relative voltage	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
VCC	Maximum supply voltage	-0.3	25	V
V_{IN}	Maximum input voltage (HIN1,2,3/LIN1,2,3)	-0.3	10	V
VG	LDO switch enable pin	0	14	V
PGND	Power ground	-1.2	1.2	V
dVS/dt	Maximum slew rate of offset voltage	-	50	V/ns

Table 8 ESD Characteristics

Symbol	Description	Min	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	-	1000	V

Note: The 100pF capacitor is discharged through a 1.5kΩ resistor.

4.3 Electrical characteristic parameters

T_A=25℃, VCC=$VBS_{1,2,3}$=15V, $VS_{1,2,3}$=GND; all pins take GND as the reference points, unless otherwise specified.

Table 9 Supply Voltage Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VBS_{HY+}	VBS undervoltage high-level potential	4.0	4.3	4.6	V
VBS_{HY-}	VBS undervoltage low-level potential	3.7	4.0	4.3	V
VBS_{HY}	VBS undervoltage hysteresis level	0.2	0.3	0.4	V
VCC_{HY+}	VCC undervoltage high-level potential	4.5	4.6	4.75	V
VCC_{HY-}	VCC undervoltage low-level potential	4.25	4.35	4.45	V
VCC_{HY}	VCC undervoltage hysteresis level	0.15	0.25	0.3	V

Table 10 Supply Current Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CCD}	VCC dynamic current	$f_{LIN1,2,3}$=20kHz	700	1350	2000	uA
I_{BSD}	VBS dynamic current	$f_{HIN1,2,3}$=20kHz	100	150	400	uA
I_{CCQ}	VCC quiescent current	V_{IN}=0V	700	950	1200	uA
I_{BSQ}	VBS quiescent current	V_{HIN}=0V	30	50	80	uA
I_{LK}	VB floating power supply leakage current	VB=225V	0	0.1	5	uA

Table 11 Time Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ON}	Output rising edge transmission time	No Load	160	270	350	ns
t_{OFF}	Output falling edge transmission time	No Load	160	270	350	ns
t_r	Output rise time	C_L=3.3nF	55	90	110	ns
t_f	Output fall time	C_L=3.3nF	40	60	90	ns
DT	Dead time	No Load	300	500	650	ns
MT	High and low-side matching time	No Load	0	20	50	ns
tLDO_ON	LDO enable transmission time		300	400	700	ns
tLDO_OFF	LDO disable transmission time		300	400	700	ns

Table 12 Input-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN+}	Input high-level potential		1.70	2.15	2.40	V
V_{IN-}	Input low-level potential		0.65	1.45	1.85	V
I_{IN+}	Input high-level current	V_{IN}=5V	8	11	15	uA
I_{IN-}	Input low-level current	V_{IN}=0V	-1	0	1	uA
V_{INHY}	Input hysteresis level		0.45	0.7	1.1	V

Table 13 Driver output-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT+}	High-level output voltage	I_{OUT}=100mA 15V- V_{OUT}	-	0.51	-	V
V_{OUT-}	Low-level output voltage	I_{OUT}=100mA V_{OUT}-GND	-	0.18	-	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA 15V- V_{OUT}	0.05	0.07	0.1	V
V_{OUT-}	Low-level output voltage	I_{OUT}=10mA V_{OUT}-GND	0.02	0.04	0.08	V
I_{OUT+}	High-level short-circuit pulse current	V_{IN}=5V V_O=0V PWD≤10μs	0.7	0.9	1.2	A
I_{OUT-}	Low-level short-circuit pulse current	V_{IN}=0V V_O=15V PWD≤10μs	0.9	1.1	1.5	A

Table 14 Built-in LDO parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
V_{LDO}	LDO output voltage	VCC=5~20V, Iload=1mA~60mA	3.23	3.3	3.37	V
ΔV_{LDO_LOAD}	Load adjustment	VCC=15V, Iload=0.1mA~33mA	-	20	40	mV
ΔV_{LDO_LOAD}	Load adjustment	VCC=5V, Iload=0.1mA~33mA	-	30	60	mV
ΔV_{LDO_VCC}	Power adjustment	VCC=4~20V, Iload=0.1mA	-	10	20	mV
ΔV_{LDO_VCC}	Power adjustment	VCC=4~20V, Iload=33mA	-	15	30	mV
PSR	Power suppression	Feq=10kHz, VCC=15V, CL=10uF	50	60	-	dB
ΔV_{LDO_TEMP}	Temperature drift	Iload=1mA, -40℃~105℃	-	50	100	mV

Parameter	Symbol	Condition	Min	Typ	Max	Unit
I_{INIT_LIMIT}	Output startup current limiting	Vout<0.7V	15	25	40	mA
I_{OUT_LIMIT}	Maximum output current limiting	VCC=15V	70	100	130	mA
OTP_{HY+}	High temperature protection threshold	VCC=15V	147	151	157	℃
OTP_{HY-}	Low temperature protection threshold	VCC=15V	120	125	131	℃
OTP_{HY}	Temperature protection hysteresis	VCC=15V	21	27	33	℃
Cload	Load capacitance		4.7	10	100	uF
ESR	Equivalent series resistance		0	0	1	Ω

5 Description of application

5.1 Recommended application circuit diagram

Figure 3 Application Circuit

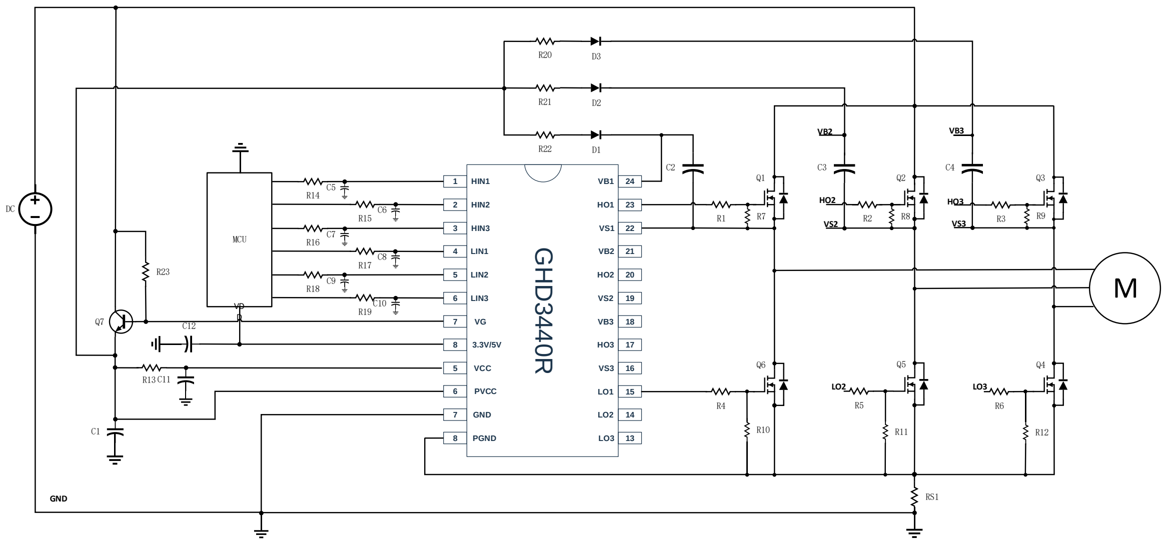


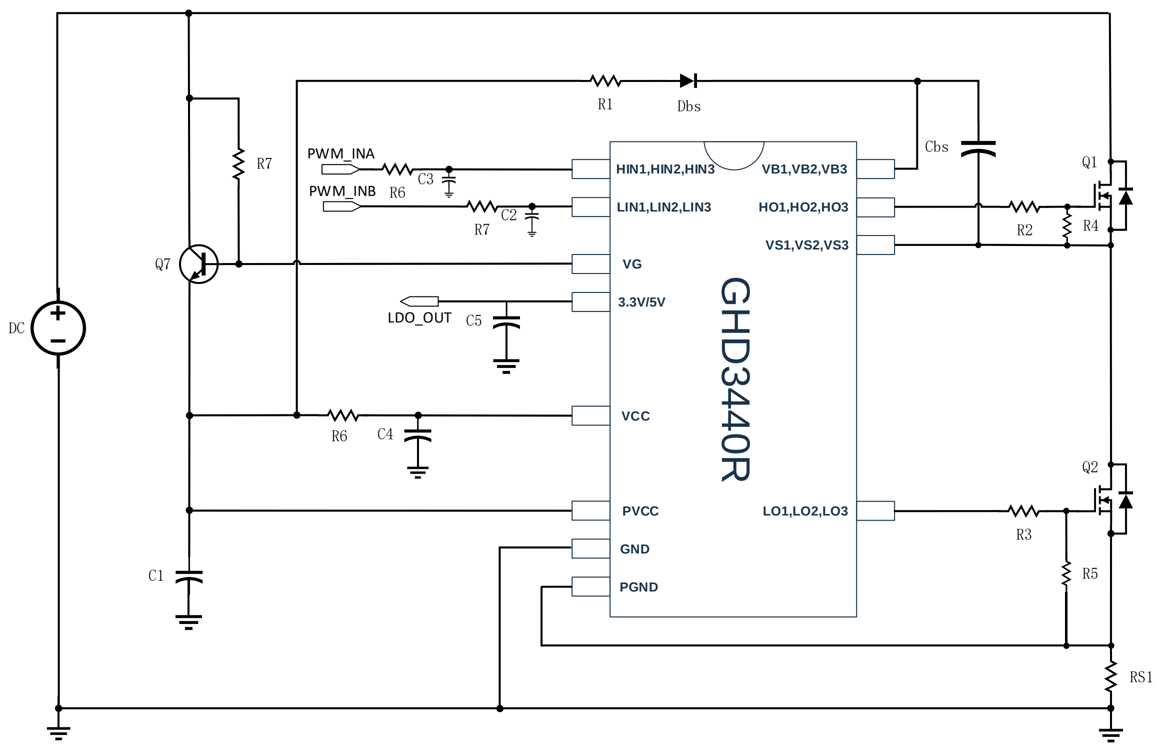
Table 15 Recommended Parameters

Designation	Typical Application Value	Remarks
C1, C11	10uF/25V/X7R/1206	Power Capacitor: Selecting a capacitor with a larger capacitance value ensures power stability.
R13	10Ω/1206	Power Divider Resistor: Select based on factors such as temperature rise and low voltage in practical applications.
R14, R15, R16, R17, R18, R19	100Ω/0603	Signal Filtering Resistor: Select based on measured signal waveform and practical application.
C5, C6, C7, C8, C9, C10	100pF/X7R/0603	Signal Filtering Capacitor: Select based on measured signal waveform and practical application.
R20, R21, R22	10Ω/0805	Bootstrapping Current Limiting Resistor: Select based on bootstrapping capacitance value, switching frequency, and other factors.
C2, C3, C4	10uF/25V/X7R/1206	Bootstrapping Capacitor: Select based on actual power transistor and switching frequency.
R1, R2, R3, R4, R5, R6	10Ω/0603	Drive Resistor: Select based on actual power transistor and Vgs drive waveform.
R7, R8, R9, R10, R11, R12	30KΩ/0603	Gate Bias Resistor: Determine whether to retain based on actual application requirements.
D1, D2, D3	Depending on actual application	Bootstrapping Diode: Select a diode with a shorter recovery time based on factors such as voltage

Designation	Typical Application Value	Remarks
		margin and overcurrent capacity in practical applications.
Q1, Q2, Q3, Q4, Q5, Q6	Depending on actual application	Power Transistor: Select based on practical application, considering voltage margin and overcurrent capacity.
RS1	Depending on actual application	Sampling Resistor: Select based on factors such as error, temperature drift, and power margin in practical applications.
C12	10uF/10V/X7R/0805	LDO Load Capacitor: It is better to select a model with a smaller equivalent series resistance (ESR).
Q7	BCP55	Step-down NPN Transistor: Select based on factors such as power supply range and power consumption.
R23	10KΩ/0805	Bias Resistor for Step-down Transistor: Select based on factors such as power supply range and power consumption.

5.2 PCB layout suggestions

Figure 4 PCB Layout Schematic Circuit



（1） The chip-powered filter capacitor C1 is placed nearby between the GHD3440R VCC pin and GND pin, and the bootstrap current limiting resistor R1, bootstrap diode Dbs, and bootstrap capacitor Cbs are placed nearby at the corresponding pin of GHD3440R to minimize the circuit area.

（2） Minimize the routing between the MCU PWM output and the GHD3440R PWM input as much as possible, and place the R6, C3, R7, and C2 filter resistors and capacitors close to the GHD3440R pin.

（3） Place the driving gate resistor R2, R3, and gate pull-down resistors R4, R5 close to the Q1 and Q2 gates to reduce the oscillation caused by the routing inductor to the driving signals.

（4） The area of the power circuit should be as small as possible, and the power ground, power ground, and signal ground should be routed separately.

（5） If a DC-DC switching power supply is used in the circuit, the operating frequency of the DC-DC circuit should be high, and the circuit area should be as small as possible. It is best to arrange this part according to the recommended layout for the used DC-DC chip.

（6） The power circuit area should be as small as possible, and the power ground, power ground, and signal ground should be wired separately.

（7） If a DC-DC switching power supply is used in the circuit, the operating frequency of the DC-DC circuit should be relatively high, and the circuit area should also be as small as possible. Please refer to the recommended layout of the DC-DC chip used for this layout.

5.3 Selection of peripheral devices

（1） The bootstrap capacitor with low ESR is recommended, with a voltage resistance of 2*VCC or above, and a capacitance value within 1u~100uF. It shall be select based on the actual observed ripple, and be used in conjunction with a clamping diode.

（2） The bootstrap diode with fast recovery is recommended, with a voltage resistance of 2*VIN or above and an instantaneous current value greater than 1A. It shall be used in conjunction with a current limiting resistor according to the actual power-on and charging time.

（3） The driving resistance is determined by the parameters of the driven device, dead time, MOSFET power consumption, and electromagnetic compatibility. It is recommended to use the backward diode or PNP triode to quickly turn off the circuit.

（4） The LDO load capacitor C5 has the function of stabilizing the loop. It is recommended to use a capacitor between 10uF and 100uF, and it is recommended to choose a capacitor with a smaller equivalent ESR. The smaller the ESR value, the smaller the ripple.

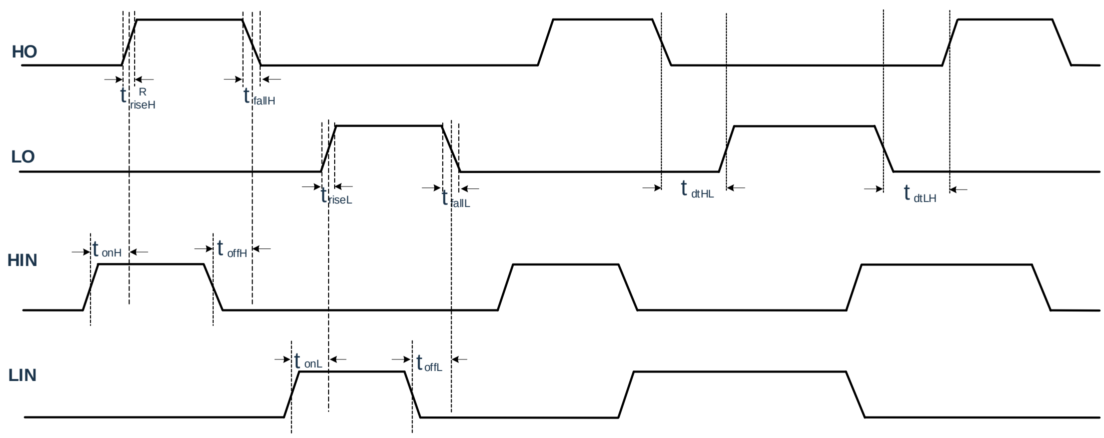
（5） The external step-down power supply Q7 is suitable for applications with 4 to 7 series lithium batteries. This solution is suitable for low-cost applications. Otherwise, it is recommended to use an independent power chip to power the driver.

6 Test instructions

6.1 Time parameter test

The time parameters mainly include the output rise time t_{rise}, the output fall time t_{fall}, the rising edge transmission time t_{on}, the falling edge transmission time t_{off}, and the dead time t_{dt}.

Figure 5 Time Parameters



6.2 VCC and VBS undervoltage test

VCC and VBS are the power supply ends of low/high circuit, respectively.

To prevent abnormal operation caused by low driving voltage and ensure that the chip operates within an appropriate supply voltage range, an undervoltage locking circuit is embedded. The VCC undervoltage high and low values falls into the level trigger category, the VBS undervoltage high value falls into the edge trigger category, the HIN edge retrigger is required, and the VBS undervoltage low value falls into the level trigger type.

Figure 6 VCC Undervoltage Timing Diagram (ignoring transmission delay)

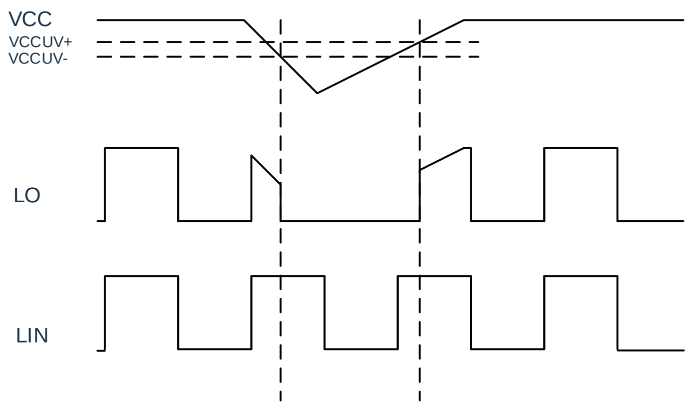
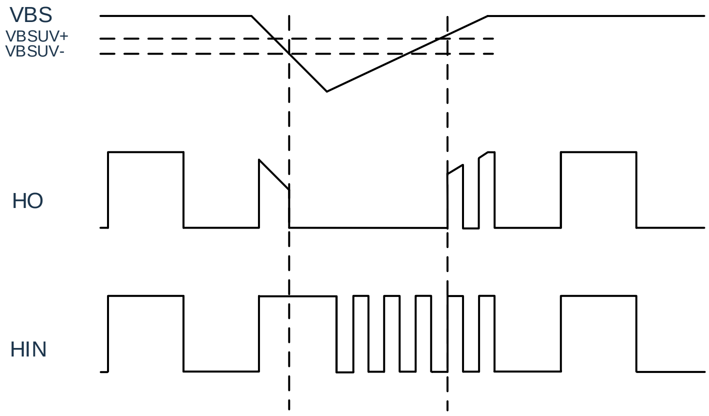


Figure 7 VBS Undervoltage Timing Diagram (ignoring transmission delay)

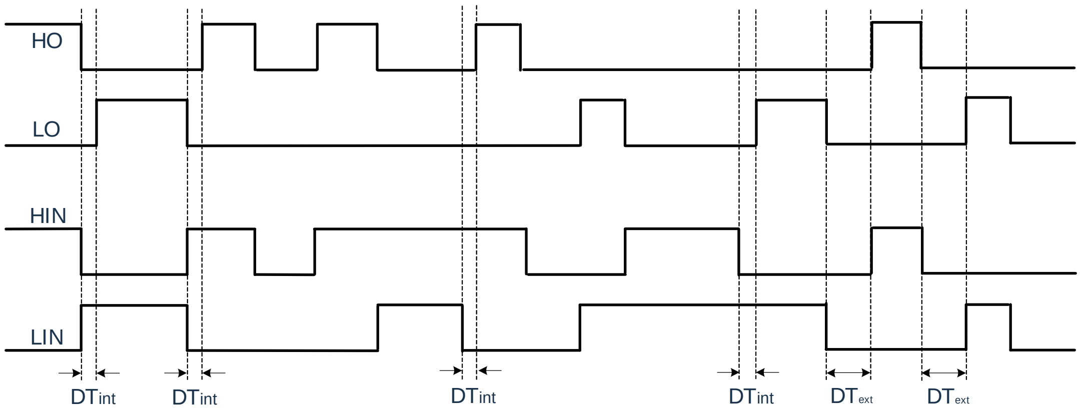


6.3 Straight-through protection and dead time test

A straight-through protection and dead time protection circuit based on the input signal is embedded in the chip. The double high level on the input logic will be determined as a straight-through signal, and the corresponding output will be set to low; moreover, it ensures that at least one dead time is embedded between the output high levels under any input condition. The logic of the external dead time DT_{ext} given on the input end and the embedded dead time DT_{int} is as follows:

- If $T_{ext}>DT_{int}$, $DT=DT_{ext}$
- If $DT_{ext}<DT_{int}$, $DT=DT_{int}$

Figure 8 Logic Timing Diagram (ignoring transmission delay)



7 Package information

7.1 Package Identification

Figure 9 Package Identification

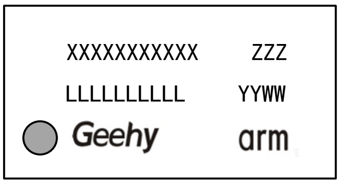


Table 16 Silkscreen Diagram Description

Symbols and Icons	Description
Geehy	Geehy
XXXXXXXXXXX	Product Model
ZZZ	Version number
YYWW	Year and week
arm	Arm® Licensed trademark
●	PIN1 Location

7.2 SSOP24 package diagram

Figure 10 SSOP24 Package Diagram

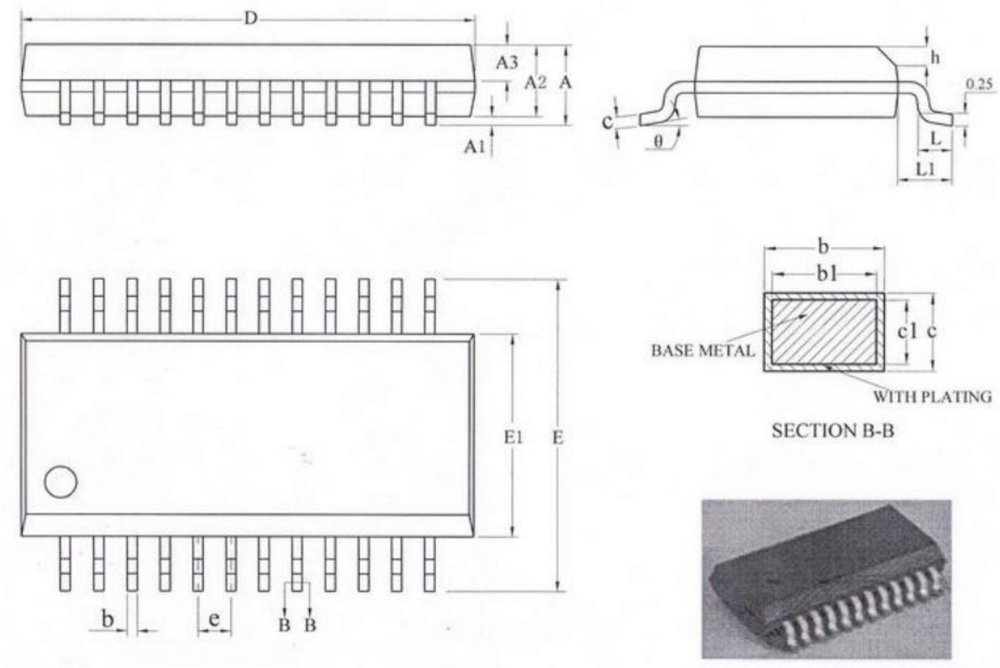


Table 17 SSOP24 Package Data

Symbol	Millimeter		
	Min	Nom	Max
A	–	–	1. 75
A1	0. 10	0. 15	0. 25
A2	1. 30	1. 40	1. 50
A3	0. 60	0. 65	0. 70
b	0. 23	–	0. 31
b1	0. 22	0. 25	0. 28
c	0. 20	–	0. 24
c1	0. 19	0. 20	0. 21
D	8. 55	8. 65	8. 75
E	5. 80	6. 00	6. 20
E1	3. 80	3. 90	4. 00
e	0. 635BSC		
h	0. 30	–	0. 50
L	0. 50	–	0. 80
L1	1. 05REF		
θ	0	–	8°

Note:

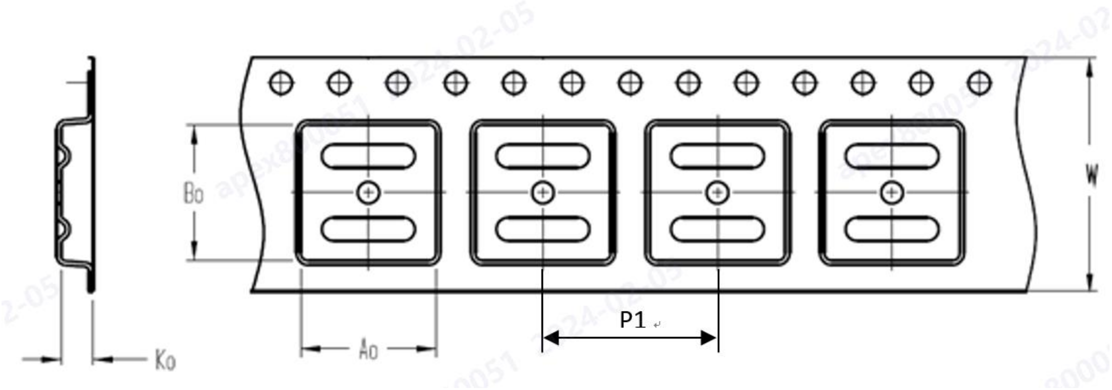
（1）Dimensions are marked in millimeters

（2）BSC is a unit without error, which refers to millimeter here

8 Packaging information

8.1 Reel package

Figure 11 Tape and Reel Packaging Specification Diagram



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
P1	Dimension designed to accommodate the component pitch
W	Overall width of the carrier tape

Figure 12 Quadrant Assignment of PIN1 Orientation in Tape and Reel

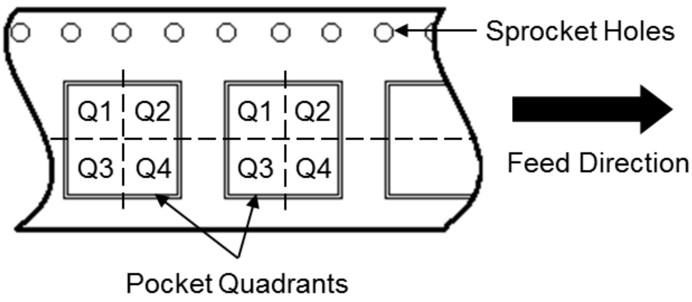


Figure 13 Reel Dimensions

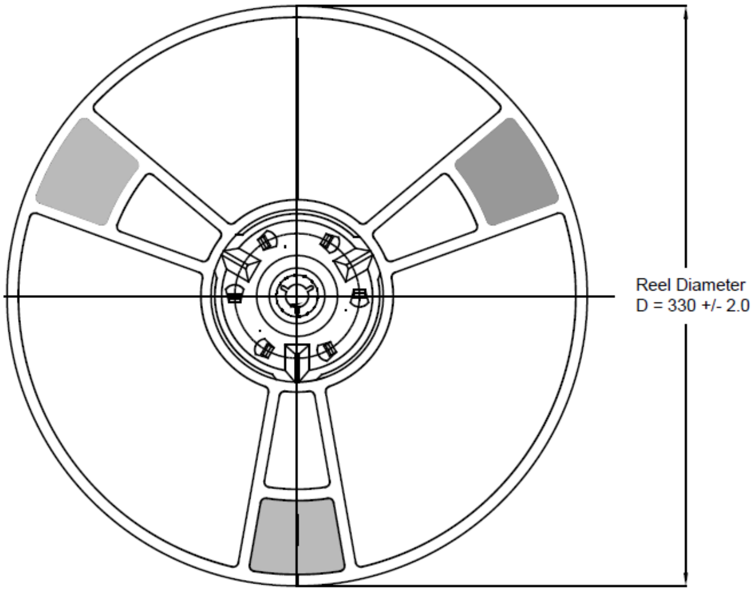


Table 18 Tape and Reel Packaging Specifications

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	P1 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
GHD3440R	SSOP	24	8000	330	6.60	9.15	8	1.80	16.00	Q1

9 Ordering information

Table 19 Ordering Information Table

Product model	Package	Packaging
GHD3440R	SSOP24	Reel

10 Revision history

Table 20 Document Revision History

Date	Version	Revision History
June, 2025	V1.0	New

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.